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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,284	01/28/2004	Takuya Daishin	450100-04892	3455

7590 04/24/2007

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EXAMINER	
GUARINO, RAHEL	
ART UNIT	**PAPER NUMBER**
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/766,284	DAISHIN ET AL.	
	Examiner	Art Unit	
	Rahel Guarino	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/28/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because:

Page 14 line 17, "203 is **outputted** to the A/D converter 103" should be "203 is **inputted** to the A/D converter 103".

Page 15 line 5, "from the A/D converter 103 **outputted** to the first equalizer 301" should be "from the A/D converter 103 **inputted** to the first equalizer 301".

Page 15 line 7, "from the first equalizer 301 is **outputted** to the second equalizer 302" should be "from the first equalizer 301 is **inputted** to the second equalizer 302".

Page 15 line 9, "from the phase frequency controller 202 is **outputted** to the voltage controlled oscillator 203" should be "from the phase frequency controller 202 is **inputted** to the voltage controlled oscillator 203".

Correction is required. See MPEP § 608.01(b).

Drawings

2. **Figure 7 and 8 should be designated by a legend such as --Prior Art--** because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1, 2, 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yada US 5,526,200 in view of Honna US 6,671,244.

Re claim 1, a reproduced signal waveform processing apparatus (fig.2), comprising: a feedback loop comprising

sampling means ((11), "ADC") for sampling a reproduced signal at an interval of a reproducing clock signal generated at a predetermined oscillation frequency (col. 3 line 43-51 and col. 6 line 64-67 for sampling; (VCO,17) col. Line 7 line 27-32);

a first equalizer (12) for equalizing a digital reproduced signal obtained by the sampling means (col. 6 line 67 to col. 7 line 1);

phase frequency control (phase comparator, 14) means for detecting a phase error at a frequency between the digital reproduced signal equalized in the first equalizer and the reproducing clock signal (col. 7 line 12-17 and col. 4 line 55-61), and outputting a control signal in accordance with phase frequency error information between the digital reproduced signal and the reproducing clock signal (col. 3 line 5-8

and the phase comparator outputs signal P(k) after comparing digital samples S(k), signal from pattern detector (19), (col. 7 line 45-57); and

oscillation (VCO (17) means for varying a oscillation frequency in accordance with an instruction from the phase frequency control means (based on output P(k) from the phase comparator, the VCO a control voltage that oscillates ADC, (col. 27-32 and col. 3 line 5-11);

wherein the feedback loop is a synchronization circuit ((ADC (11), equalizer (12), phase comparator (14) thru pattern detector (19) including PLL controller (18)) that functions as a phase locked loop (PLL) for synchronizing frequency phase between the digital reproduced signal and the reproducing clock signal (col. 4 line 2-6 and col. 7 line 18-27), does not teach a second equalizer.

However, Honna teaches adaptive equalizer (fig.2, 32, col. 3 line 13-15). By arranging equalizer (1) from Yoda with equalizer (2) from Honna, the apparatus as claimed in claim 1 will have equalizers in series, wherein the reproduced signal waveform processing apparatus further comprises a second equalizer connected in series with the first equalizer.

Therefore, taking the combined teaching of Yada and Honna as a whole would have been rendered obvious to one skilled in the art to modify Yada to utilize a second equalizer for the benefit of correcting error date (col. 9 line 8-10).

Re claim 2, the combined teaching of Yada and Honna according to claim 1, wherein the second equalizer means comprises an adaptive equalizer (col. 3 line 13-15 and col. 7 line 31-33," Honna") having an automatic equalization function

(col. 3 line 39-46, "Honna").

Re claim 4, the combined teaching of Yada and Honna according to claim 1, wherein the phase frequency (fig. 6; phase comparator, 14) control means comprises a FIR filter (col. 8 line 28-30, "Yada").

Re claim 7, the combined teaching of Yada and Honna according to claim 1, wherein the sampling means is an analog/digital converter (fig.2, (ADC;11), col. 6 line 64-66, col. 7 line 12-14, "Yada").

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 3 and 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yada, US 5,526,200 in view of Honna US 6,671,244 and in further view of Kishi US 5,148,382.

Re claim 3, the combined teaching of Yada and Honna according to claim 1 discloses the first equalizer, does not teach the equalizer comprising an IIR filter.

However, Kishi teaches an equalizer (IIR filter (36)), (fig.1, col. 2 line 21-36).

Therefore, taking the combined teaching of Yada and Honna and Kishi as a whole would have been rendered obvious to one skilled in the art to modify Kishi to

utilize the equalizer (IIR filter) for the benefit of suppression of cycle noises (col. 5 line 46-48).

Re claim 5, the combined teaching of Yada and Honna according to claim 1, does not teach the operating clock of feedback loop functioning at a frequency of the Second equalizer's operating clock.

However, Kishi teaches a sampling frequency generated by the sampling clock (40) that activates the ADC (34), (fig.1, (col. 3 line 36-40).

Therefore, taking the combined teaching of Yada and Honna and Kishi as a whole would have been rendered obvious to one skilled in the art to modify Kishi to utilize the operating clock of the feedback loop for the benefit of avoiding tuning circuitry (col. 6 line 17-21,"Kishi").

Allowable Subject Matter

7. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rahel Guarino whose telephone number is 571-270-1198. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Payne David can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RG

David Payne

DAVID C. PAYNE
SUPERVISORY PATENT EXAMINER